An external clock driver circuit that provides a two-phase clock (two clock signals 180° out of phase with respect to each other) is required for the original 6800. Motorola simplified the design of 6800-based computer systems by introducing two variants, the 6802 and 6808. The 6802 includes an on-board clock driver circuit of the type that is now standard on many microprocessors available today. Such clock drivers require only an external *crystal* to create a stable, reliable oscillator with which to clock the microprocessor. A crystal is a two-leaded component that contains a specially cut quartz crystal. The quartz can be made to resonate at its natural frequency by electrical stimulus created within the microprocessor's on-board clock driver circuitry. A crystal is necessary for this purpose, because its oscillation frequency is predictable and stable. The 6802 also includes 128 bytes of on-board RAM to further simplify certain systems that have small volatile memory requirements. For customers who wanted the simplified clocking scheme of the 6802 without paying for the on-board RAM, Motorola's 6808 kept the clocking and removed the RAM.

Using a 6802 with its internal RAM, a functional computer could be constructed with only two chips: the 6802 and an EPROM. Unfortunately, such a computer would not be very useful, because it would have no I/O with which to interact with the outside world. Motorola manufactured a variety of peripheral chips intended for direct connection to the 6800 bus. Among these were the 6821 peripheral interface adapter (PIA) and the 6850 asynchronous communications interface adapter (ACIA), a type of UART. The PIA provides 20 I/O signals arranged as two 8-bit parallel ports, each with two control signals. Applications including basic pushbutton sensing and LED driving are easy with the 6821. The 6800 bus uses asynchronous control signals, meaning that memory and I/O devices do not explicitly require access to the microprocessor clock to communicate on the bus. However, many of the 6800 peripherals require their own copy of the clock to run internal logic.

As with all synchronous logic, the 6800's bus is internally controlled by the microprocessor clock, but the nature of the control signals enables asynchronous read and write transactions without referencing that clock, as shown in Fig. 6.2. An address is placed onto the bus along with the proper state of the R/W select signal (read = 1, write = 0) and a valid memory address (VMA) enable that indicates an active bus cycle. In the case of a write, the write data is driven out some time later. For reads, the data must be returned fast enough to meet the microprocessor's timing specifications. The 6802/6808 were manufactured in 1-, 1.5-, and 2-MHz speed grades. At 2 MHz, a peripheral device has to respond to a read request with valid data within 210 ns after the assertion of address, R/W, and VMA. A peripheral has up to 290 ns from the assertion of these signals to complete a write transaction.* In a real system, VMA, combined with address decoding logic, would drive the individual chip select signals to each peripheral.

In some situations, slow peripherals may be used that cannot execute a bus transaction in the time allowed by the microprocessor. The 6800 architecture deals with this by stretching the clock during

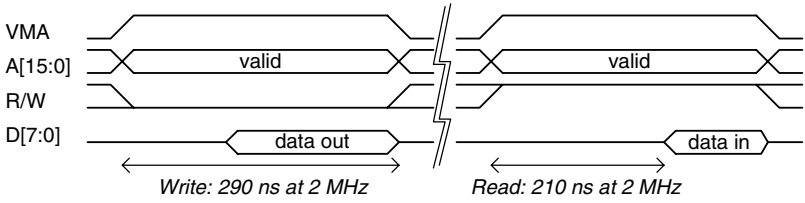

FIGURE 6.2 6802/6808 basic bus timing.

* *8-Bit Microprocessor and Peripheral Data,* Motorola, 1983, pp. 3–182.

a slow bus cycle. A clock cycle can be stretched as long as 10 μs, enabling extremely slow peripherals by delaying the next clock edge that will advance the microprocessor's internal state and terminate a pending bus cycle. This stretching is performed by an external clock circuit for a 6800, or by the internal clock of the 6802/6808. As with many modern microprocessors, the 6802/6808 provides a pin that delays the end of the current bus cycle. This memory ready (MR) signal is normally high, signaling that the addressed device is ready. When brought low, the clock is internally stretched until MR goes high again. Early microprocessors such as the 6800 used clock stretching to delay bus cycles. Most modern microprocessors maintain a constant clock frequency and, instead, insert discrete *wait states*, or extra clock cycles, into a bus transaction when a similar type of signal is asserted. This latter method is usually preferable in a synchronous system because of the desire to maintain a simple clock circuit and to not disrupt other logic that may be running on the microprocessor clock.

Motorola's success with the 6800 motivated it to introduce the upgraded 6809 in 1978. The 6809 is instruction set compatible with the 6800 but includes several new registers that enable more flexible access to memory. Two stack pointers are present: the existing hardware controlled register for subroutine calls and interrupts, and another for user control. The user stack pointer can be used to efficiently pass parameters to subroutines as they are called without conflicting with the microprocessor's push/pop operations involving the program counter and other registers. A second index register and the ability to use any of the four 16-bit pointer registers as index registers were added to enable the simultaneous handling of multiple data structure pointers without having to continually save and recall index register values. The 6809's two accumulators can be concatenated to form a 16-bit accumulator that enables 16-bit arithmetic with an enhanced ALU. This ALU is also capable of eight-bit unsigned multiplication, which made the 6809 one of the first integrated microprocessors with multiplication capability.

Other improvements in the 6809 included a direct page register (DPR) for a more flexible eight-bit direct addressing mode. The 8-bit DPR, representing A[15:8], is combined with an 8-bit direct address, representing A[7:0], to form a 16-bit direct address, thereby enabling an 8-bit direct address to reference any location in the complete 64-kB address space. The 6809 also included a more advanced bus interface with direct support for an external DMA controller. Several desktop computers, including the Tandy/Radio Shack TRS-80 Color Computer, and various platforms, including arcade games, utilized the 6809.

While still available from odd-lot retail outlets, the original 6800 family members are no longer practical to use in many computing applications. Their capabilities, once leading edge, are now available in smaller, more integrated ICs at lower cost and with lower power consumption. However, the 6800 architecture is alive and well in the 68HC05/68HC08 and 68HC11 microcontroller families that are based on the 6800/6802/6808 and 6809 architectures, respectively. These microcontrollers are available with a wide range of integrated features with on-board RAM, ROM (mask ROM, EEPROM, or EPROM), serial ports, timers, and analog-to-digital converters.

6.3 INTEL 8051 MICROCONTROLLER FAMILY

Following their success in the microprocessor market, Intel began manufacturing microcontrollers in 1976 with the introduction of the 8048 family. This early microcontroller contains 64 bytes of RAM, 1 kB of ROM, a simple 8-bit microprocessor core, and an 8-bit timer/counter as its sole on-board peripheral. (Subsequent variants, the 8049 and 8050, include double and four times the memory of the 8048, respectively.) The microprocessor consists of a 12-bit program counter, an 8-bit accumulator and ALU, and a 3-bit stack pointer. The 8048 is a complete computer on a single chip and gained a certain amount of fame in the 1980s when it was used as the standard keyboard controller on the